The Amplifier

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**Objective**

The purpose of this lab is to illustrate and reinforce operational and modeling concepts of metal-oxide-semiconductor field-effect transistors (MOSFETs) used as analog amplifiers. This will be accomplished by creating a single-stage amplifier through the design of a Common Source amplifier with Source Resistor to meet specifications. This will be followed by the creation of a cascaded amplifier through the design of a Common Source amplifier with Source Resistor cascaded with a Common Drain amplifier to meet specifications.

**Specifications and Limitations**

Single Stage Amplifier:

- Circuit Topology: Common-source with source resistor (See Fig. 1 for topology)

- Transistor: BS-170 MOSFET

- VDD from 10 to 20 V (10V ≤ VDD ≤ 20V)

- Maximum drain current: 75% of the max transistor DC current (from data sheet)

- Input Resistance (Ri): > 100 kΩ

- Output Resistance (Rout): ≤ 5 kΩ

- Load Resistance (RL): 100 kΩ (AC-coupled using 10 µF - 47µF electrolytic capacitor)

- vin: 1kHz sine wave – AC-coupled (10μF - 47μF electrolytic capacitor)

- Voltage Gain (Av): −3 V/V ≥ AV ≥ −30 V/V (no visible signal distortion)

- vout: Should achieve at least 3 Vp-p with no visible distortion

- Instantaneous power dissipation in any part not to exceed 75% of max power dissipation

- Potentiometers may not be used for any part of the design

Cascaded Amplifiers:

- Circuit Topology: Common-source with source resistor cascaded with a common-drain (See Fig. 2 for topology).

- Transistor: BS-170 and BS-250

- VDD from 10 to 20 V (10V ≤ VDD < 20V)

- Maximum drain current: 75% of the max transistor DC current (from data sheet)

- Input Resistance (Ri): Ri > 100 kΩ - Ri of the PMOS > 100 kΩ

- Output Resistance (Rout): Rout ≤ 5 kΩ

- Load Resistance (RL): 50 Ω (AC coupled using 10 µF–47µF electrolytic caps)

- vin : 1kHz sine wave -- AC coupled (10μF – 47μF Electrolytic cap)

- Voltage Gain ( AV ): -3 V/V ≥ AV > -30 V/V (no visible signal distortion)

- vout: The amplifier should be able to supply at least 3 Vp-p with no visible distortion

- Instantaneous power dissipation in any part may not exceed 75% of max power dissipation specified for the part

- Potentiometers may not be used for any part of the design.

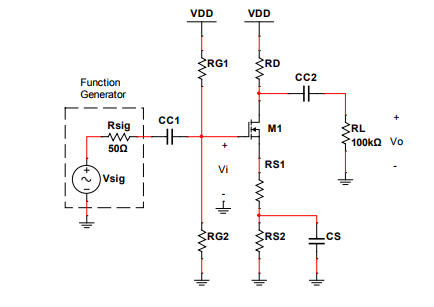
- VSD of PMOS ~7 Volts (or roughly ½ the supply voltage)

- ID of PMOS ~60 mA

**General Approach**

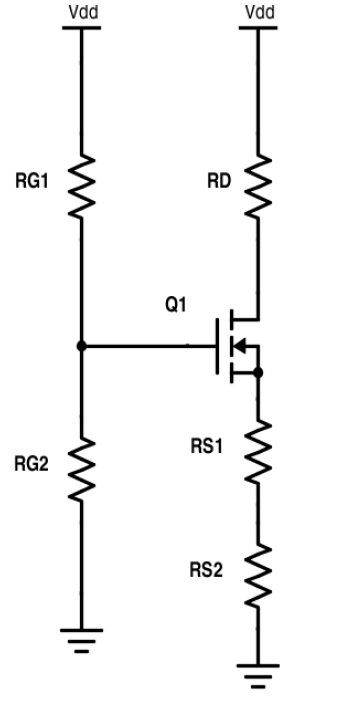
The amplifier lab was broken up into two parts: single stage amplifier and cascaded amplifier. The laboratory experiment began with building a single stage amplifier that produces a gain between -3 V/V and -30 V/V. The second part of the lab was an extension of single stage amplifier by adding a cascaded amplifier. This buffering circuit had to produce a gain near 1 V/V. The best approach to the amplifier lab is to build the two parts separately and making sure that each part worked as expected. These two circuits were first designed and simulated in MultiSim before experimenting them on the lab using actual components.

For the single stage amplifier, the lab instruction specifies to build a common-source amplifier with a source resistor using a NMOS transistor to produce a gain between -3 V/V and -30 V/V. Before simulating or experimenting, governing equations are needed to come up with a design that will meet the specifications needed to produce the gain. Figure 1 illustrates the common-source amplifier using an NMOS transistor.



**Figure 1.** Common-source amplifier with source resistor using NMOS FET biased with the classical 4- resistor scheme.

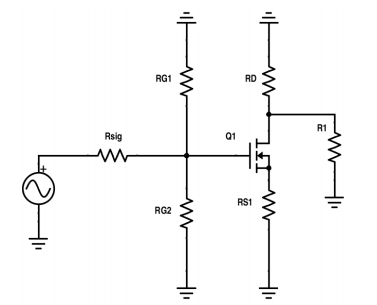
Using the general schematic provided above, a set of governing equations were needed to help determine the values of the components to meet the specifications of the single stage amplifier. First, a large signal model (Figure 2) was used to determine the governing equations for VG, VS, VD, and ID. When using a large signal model, the components of the circuits that are affected by that signal has to be isolated. When using a large signal model, the capacitors that are connected in the gate, source, and drain are considered or seen as open. Now that the large signal model has isolated the components, VDD is used to create a biasing scheme to determine how VDD will be divided amongst the RD, VDS, and the RS. A method from class that was used to disperse VDD is the 40%, 40%, 20% rule. About 40% of VDD is dropped across RD, 40% across RS, and the remaining 20% on VDS. VG will be determined after finding VD and VS using the biasing scheme.

**Figure 2.** The Large Signal model for Single Stage Amplifier

Large Signal Equations:

The specification of Rout is less than or equal to 5kΩ. Since Rout is about that same as RD, the value of RD was determined to be 4.7kΩ. The specification states that the value of VDD has to be between 10 to 20V. For all calculation, simulation, and experiment, the value of VDD was set to 15V. Subtracting the VDD with 9V is equal to 6V. This voltage is the value of VD. Dividing the value of VD by the resistance of RD equal to the drain current ID. Using the 40%, 40%, 20% rule, the values of VD and VDS will both obtain the 40% of the total VDD and VS will have the remaining 20%. Since the value of VS have been determined by the 40%, 40%, 20% rule, VS can be divided by the ID, which will give the resistance value of RS1 plus RS2. Using Equation 4, VG can be determined. ID and VS has already been determined at this point. The values of kn and Vt are both characteristics of a NMOS transistor. According to the specifications, kn is assumed to have a value of 250 mA/V2 and Vt is assumed to have a value of 2V (this will change as we characterize the transistor using a curve tracer for the design portion of the lab). Using the value of VG solved using Equation 4, Equation 1 can be used to solve for the values of RG1 and RG2. The specification states that the value of Rin, which is equal to RG1 parallel RG2, can’t be greater than 100kΩ. The resistive value of RG1 can be determined by the designer to solve for the remaining unknown value of RG1. The overdrive voltage, VoV, is equal to the difference between VGS and Vt.

When the amplifier circuit is seen from the small signal’s perspective, the capacitors are seen as shorts, which help disregard for the large signal voltages. Small signal circuit is demonstrated in Figure 3. By analyzing Figure 3 below, small signal equations can be determined.



**Figure 3.** Small signal Model circuit of the nMOSFET in the common-source configuration

Small Signal Equations:

5)

6)

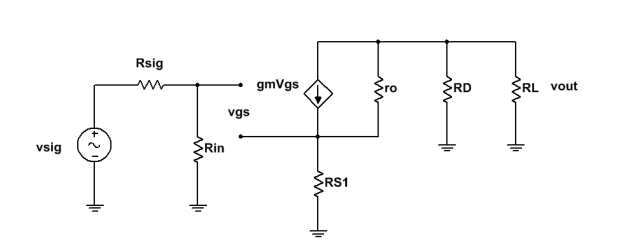
7)

8)

9)

10)

The value of gm can be determined through Equation 5. After determining the value of gm, the values of AV and AV0 can also be determined using Equation 6 and 7. The value of r0 can be disregarded when solving for the value of AV since it is in parallel with RD and RL and they have a greater magnitude than r0. The value of Gv can be solved by multiplying the gain with Rsig in parallel with Rin (Equation 8). The value of Rin is equal to RG1 in parallel to RG2 (Equation 9). Lastly, the value of Rout is equal to RD parallel to RL (Equation 10).

**Figure 4.** The hybrid-pi model of the Small Signal Operation of the nMOS FET in the common-drain configuration. 

After determining and meeting all the specification and limitations needed for the simulation portion of the amplifier lab, construct the circuit as shown in Figure 1. Make sure to build the circuit using the theoretical values for the components. In order to build a model with more accurate transistor value, signal tracer is needed to further characterize the transistor that is being used. Signal tracer will assist in analyzing the threshold voltage and value of r0 of the transistor being used. In order to calculate for the value of lambda, inverse the value of r0 found using the signal tracer. After the characterizing the transistor, modify the transistor on the simulation and insert the values from the signal tracer. In the simulation portion of the lab, determine the small AC signal input that is large enough to produce a 3 Vp-p output voltage. It has to be small enough not to cause any distortion for Vout. Measure the drain, gate, and source voltages to verify that the transistor is on and the biasing scheme is working properly. Using transient analysis, analyze Vin against Vout to verify the gain.

Measure the drain current by placing a DC current node next to the drain resistor. Calculate the AV0 by excluding the load resistor from the AV gain and measure the output voltage from the negative node of the capacitor. The value of GV can be determined measuring the output measurement similar to AV and measuring the input value from the function generator input. The value of Rin and Rout can be measured by doing some rearrangements on the circuit. The Rin value is measured by placing a test resistor that has the same value as the Rin (Equation 9) between the small signal input and the coupling capacitor. Measure the voltage difference across the resistor using an oscilloscope and divide the measured voltage by the test resistor to obtain the test current. Divide the voltage measure on the right side of the test resistor (the circuit side) by the test current, which will equal to Rin. The value of Rout is obtained by doing the opposite of the Rin value. The load resistor needs to be disconnected from the circuit and the small signal source needs to be disconnected and reconnected to where the output voltage will be measured. Connect a test resistance that’s around the 100kΩ between the small signal source and the rest of the circuit. Use an oscilloscope to measure a voltage of either side of the resistor. Divide the difference of the voltage readings by the test resistor value to obtain the test current. Divide the measured voltage on the circuit side by the test current to obtain the Rout value.

Compare the simulated circuit value against the calculated values for the single stage amplifier circuit using Table 1.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Parameter | Spec & Limits | Calcs | Sim | %Error |
| ID (mA) | ≤ 75% max transistor DC current | 1.28m | 1.23m | 3.91 |
| Avo (V/V) | N/A | N/A | -19.23 | N/A |
| Av (V/V) | -3 V/V ≥ AV ≥ -30 V/V | -19.13 | -18.91 | 1.15 |
| Gv (V/V) | N/A | N/A | -18.34 | N/A |
| Rin (kΩ) | ≥ 100 kΩ | 132.2k | 132.2k | 0 |
| Rout (kΩ) | ≤ 5 kΩ | 4.7k | 4.7k | 0 |
| PD (mW) | ≤ 75% of max power any part | 7.68m | 7.64m | 0.39 |

**Table 1.** Calculated and Simulated value comparison table

After completing the simulation portion of the lab, conduct implementation portion of the circuit on a breadboard using the simulated component values. Make sure the positive node of the capacitors is facing towards the large signal portion of the circuit. If the capacitors are not in the right orientation, then the large signal circuit can’t create an open circuit. Power supply used in the lab will produce the large signal voltage and the ground node for the amplifier circuit. Connect the power supply in the positive voltage side of the breadboard to allow multiple VDD source for the circuit. Do the same for ground. Function generator will be connected in the negative side of the CC1 capacitor. Checking for voltage on the drain, gate, and source side of the transistor is important to make sure the transistor is on.

Check to see if the circuit is performing as expected by checking for all the parameters just like how simulation parameters were measured except the drain current. The drain current in the implementation portion of the lab is done by measuring the voltage drop across RD and dividing that value by the resistive value of RD.

After measuring the implementation parameters, compare the values against the simulation values and determine the percent error. The table below is used to compare the implementation values against the simulation values.

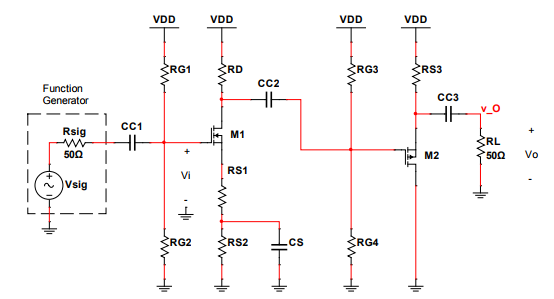
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Parameter | Spec & Limits | Sim | Lab | %Error |
| ID (mA) | ≤ 75% max transistor DC current | 1.17m | 0.88m | 24.79 |
| Avo (V/V) | N/A | -12.05 | -12.74 | 5.73 |
| Av (V/V) | -3 V/V ≥ AV ≥ -30 V/V | -11.51 | -11.71 | 1.74 |
| Gv (V/V) | N/A | -18.34 | \*Can't | Measure |
| Rin (kΩ) | ≥ 100 kΩ | 132.2k | 129.7k | 1.89 |
| Rout (kΩ) | ≤ 5 kΩ | 4.7k | 4.61k | 2.13 |
| PD (mW) | ≤ 75% of max power any part | 7.68m | 4.65m | 39.5 |

**Table 2.** Simulated and Implementation value comparison table

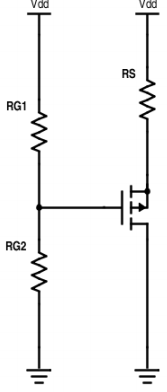
The implementation portion of the lab marks the completion of the single stage amplifier.

The second part of the amplifier lab is the Cascaded Amplifier. The Cascading amplifier should theoretically produce a gain of 1 V//V using a common drain amplifier. The Cascading amplifier allows for the load to occur across a lower load resistance. In this lab, it’ll be across a 50Ω resistor.

The design approach of common-drain amplifier is similar to common-source amplifier. It is highly recommended to design the common-drain amplifier separately from the single stage amplifier (common-source amplifier) to ensure that it works and for troubleshooting purpose.

**Figure 5.** Common-source amplifier with source resistor using NMOS FET biased with the classical 4- resistor scheme, cascaded with common-drain using PMOS FET biased with classical 4(3+1wire)-resistor scheme. 

The figure above represents the outline of the Cascading Amplifier that needs to be designed. It demonstrates how the pMOS FET with a common-drain will connected to a nMOS FET with a common-source. First, analyzing the large signal circuit is necessary to determine the large signal equations for the calculation different components. The large signal model circuit of pMOS FET in the common-drain configuration is shown in Figure 6 below.

**Figure 6.** Large Signal Model circuit of the pMOS FET in the common-drain configuration 

Large Signal Equations:

11)

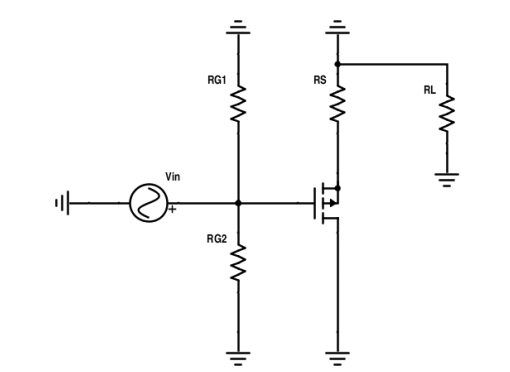
12)

13)

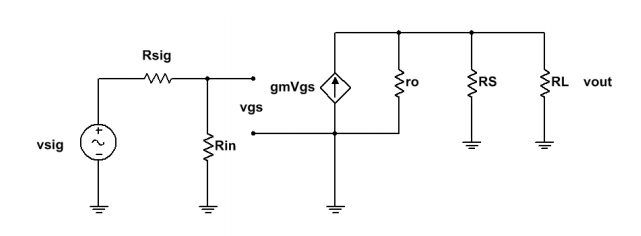
14)

Using Equation 11-15, determine the biasing scheme. Since the drain pin of the transistor is grounded, VD is measured to be 0 volt. According to the specifications and limitations, VSD has to be roughly about half of VDD. This allows VS to be calculated to be half VDD. The specification and limitation also sets the drain current of the pMOS FET to be 60 mA. This is because k and Vt have been specified to 250 mA/V^2 and -2V, so the drain current has to be set by VGS. To determine the value of RS3, subtract VDD by half of its voltage and divided by the specified drain current value of 60 mA. Using Equation 14, the value of VoV can be determined since the values of ID and k are known. After solving for VoV, VG can be determined by subtracting VSD by VoV. Using Equation 11, the values of RG3 and RG4 can be calculated. The value of RG4 can be predetermined by the designer since there will be two unknowns in equation 11. Keep in mind that RG3 has to be greater than RG4.

For the small signal circuit, the figure below shows the circuit components that are affected by the small signal input.

**Figure 7.** Small Signal Model circuit of the pMOS FET in the common-drain configuration

Using the hybrid-pi model derived from Figure 7, small signal circuit equations can be derived.

**Figure 8.** Hybrid-pi model of the Small Signal Operation of the pMOS FET in the common-drain configuration. 

Node voltage analysis is used to derive the small signal equations shown below. Resistors r0, RL and RS are in parallel with one another, and since the value of r0 will be much larger than RL and RS, r0 can be excluded from the equations to simplify the design process.

Small Signal Equations:

15)

16)

17)

18)

19)

20)

In order to determine the value of gm, Equation 15 is used. There are no unknowns in Equation 15 since K has been specified and VoV was determined earlier using Equation 14. After finding the value for gm, use Equation 16 to determine gain, Av. Note that second stage gain multiplied by the gain of the single stage amplifier is within -3 V/V to -30 V/V. Use Equation 17 to determine the value of AV0. The value of Gv is the product of AV by the ratio of Rin and Rin plus Rsig. Determine the value of RG1 and RG2 in the cascaded amplifier using Equation 19 and 20. Rin needs to be greater than 100kΩ while the Rout has to be less than or equal to 5kΩ. This concludes the calculation portion of the cascaded amplifier.

For the simulation portion of the cascaded amplifier, disconnect the 100kΩ load resistor from the single stage amplifier. Connect the output voltage to the input of the second stage of the buffer circuit. Ensure that the completed circuit works properly in the simulation. In order to get a more accurate simulation, use the signal tracer to characterize the pMOS FET. Signal tracer will assist in analyzing the threshold voltage and value of r0 of the transistor being used. In order to calculate for the value of lambda, inverse the value of r0 found using the signal tracer. After the characterizing the transistor, modify the transistor on the simulation and insert the values from the signal tracer. The Av gain of both total circuit needs to be between -3 V/V and -30 V/V and the output voltage from the amplifiers should be greater than 3 Vp-p. Using the same techniques in the single stage amplifier, measure the required parameters.

Compare the values of the parameters measured in simulation with the calculated values using the table below.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Parameter | Spec & Limits | Calcs | Sim | %Error |
| ID (mA) | ≤ 75% max transistor DC current | 60m | 56.9m | 5.16 |
| Avo (V/V) | For the CD amplifier only | N/A | 0.7705 | N/A |
| Av (V/V) | For the CD amplifier only | 0.863 | 0.7705 | 10.72 |
| Gv (V/V) | For the CD amplifier only | N/A | 0.7702 | N/A |
| Rin (kΩ) | ≥ 100 kΩ | 143k | 143k | 0 |
| Rout (kΩ) | ≤ 5 kΩ | 5.53 | 10.01 | 81 |
| PD (mW) | ≤ 75% of max power any part | 127m | 113m | 11 |

**Table 3.** Comparison of calculated circuit values to the simulated values.

For the implementation portion of the Cascaded amplifier, use the single stage amplifier and connect the buffer circuit. Use component values that are close to the one used in the simulation. Connect the two circuit by removing the load resistor from the single stage amplifier and connect the second circuit to where the output voltage of the first circuit to the input of the second circuit. Use a multimeter to ensure that the voltage in drain, source, and gate areas expected to determine if the transistor is on.

After connecting the two circuits make sure it produces a single two gain stage amplifier circuit. Start measuring the circuit parameters using the techniques used to measure the parameters in the simulation and first circuit. Make sure to compare the simulated values with the implementation values and determine the percent error to see how close the values are between them. Use the table below to record the values.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Parameter | Spec & Limits | Sim | Lab | %Error |
| ID (mA) | ≤ 75% max transistor DC current | 56.9m | 51m | 10 |
| Avo (V/V) | For the CD amplifier only | 0.7705 | 1.072 | 39.13 |
| Av (V/V) | For the CD amplifier only | 0.7705 | 0.7668 | .5 |
| Gv (V/V) | For the CD amplifier only | 0.7702 | N/A | N/A |
| Rin (kΩ) | ≥ 100 kΩ | 143k | 138.85k | 2.90 |
| Rout (kΩ) | ≤ 5 kΩ | 10.01 | 13.16 | 31.5 |
| PD (mW) | ≤ 75% of max power any part | 113m | 122m | 7.96 |

**Table 4.** Comparison of simulated circuit values to the implemented values.

**Design**

According to the lab handouts, the circuit should be designed with k = 250 mA/V^2 and Vt = 2V. These values are not completely accurate to the BS-170. The implementation values will be different, but the design will guide us toward the right approach. Using the biasing scheme outlined in the approach section with VDD equaling to 15V, the following parameters are calculated.

Biasing Scheme:

VDD = 15V

V­D = 9V, VS = 6V

Let RD = 4.7kΩ (It has to be less than or equal to 5kΩ)

Drain current was calculated by dividing 6V by RD, which came out to 1.28mA.

ID = 1.28mA:

ID = ½  k(VOV)^2

1.28 mA = ½ (250 mA/V2 )(VOV)^2

VOV = +/- 0.101V

Saturation:

1. Vov = VG − VS − Vt = 0.101 V 2) Vov = VG − VS − Vt = −0.101 V Vov = VG − 6V − 2V = 0.101 V Vov = VG − 6V − 2V = −0.101 V VG = 8.101 V VG = 7.899 V VGS = 2.101 V VGS = 1.899 V VGS > Vt VGS < Vt |VDS| > |Vov| |VDS| > |Vov| Transistor is on because VGS > Vt Transistor is off because VGS < Vt

Calculating gm:

gm = kVov

gm = (250mA/V2 )(0.101V)

gm = 25.25mA/V

Calculating AV0:

Choose Av0 = -20 V/V:

RS1 = 195Ω (Standard resistor value = 200Ω)

RS1 + RS2 = 2.35kΩ

RS2 = 2.15kΩ (Standard resistor value = 2.2kΩ)

Calculating Av:

Calculation for resistors:

Choosing RG1 and R­G2 values

Let RG2 = 200kΩ, then RG1 = 388.12kΩ

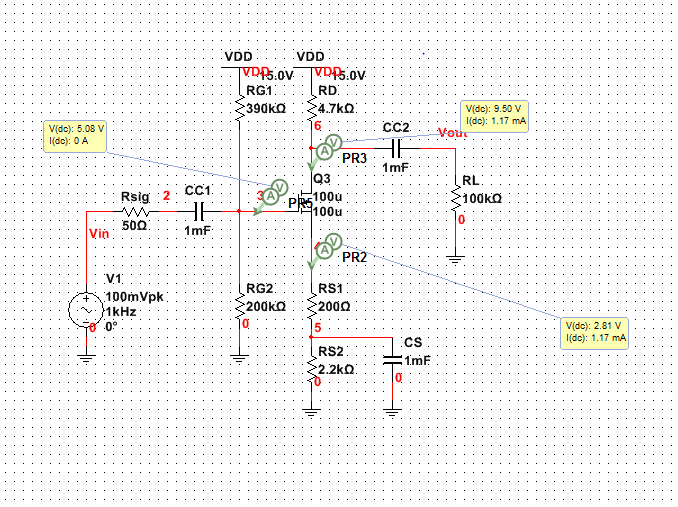
Calculating Rin: Calculating Rout:

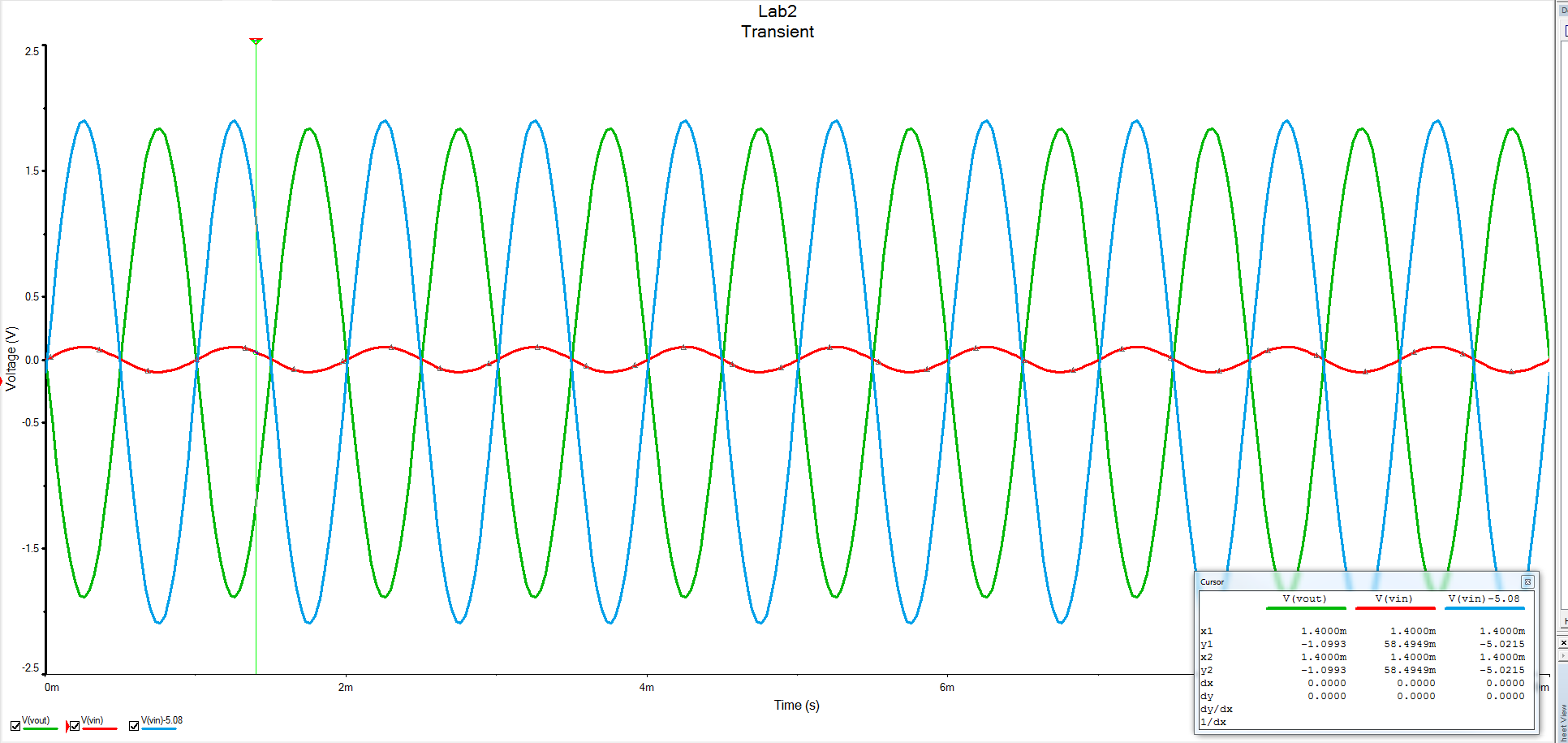
Rin = (RG1∗RG2)/(RG1+RG2) Rout = (RD∗ RL)/(RD+ RL)

Rin = (390kΩ∗200kΩ)/(390kΩ+200kΩ) Rout = (4.7kΩ∗ 100kΩ)/(4.7kΩ+ 100kΩ) Rin = 132 kΩ Rout = 4.7 kΩ

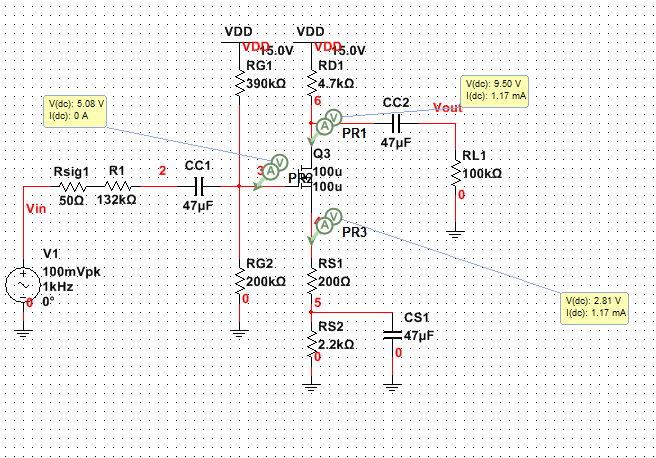
Calculating Gv:

GV = - 18.73 V/V

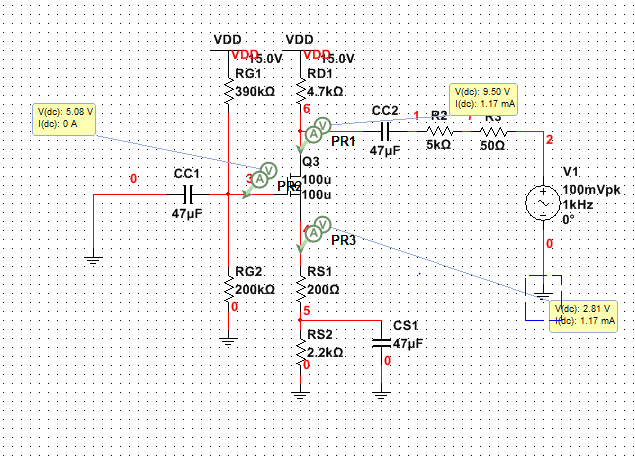
**Figure 9.** Multisim Schematic of the Single Stage Amplifier

Transient analysis needs to be performed in order to verify that the circuit meets the specifications and limitations.

**Figure 10.** Transient Analysis of the AV gain for the Single Stage Amplifier.



**Figure 11.** Circuit set up for Rin measurement of the first stage of the circuit

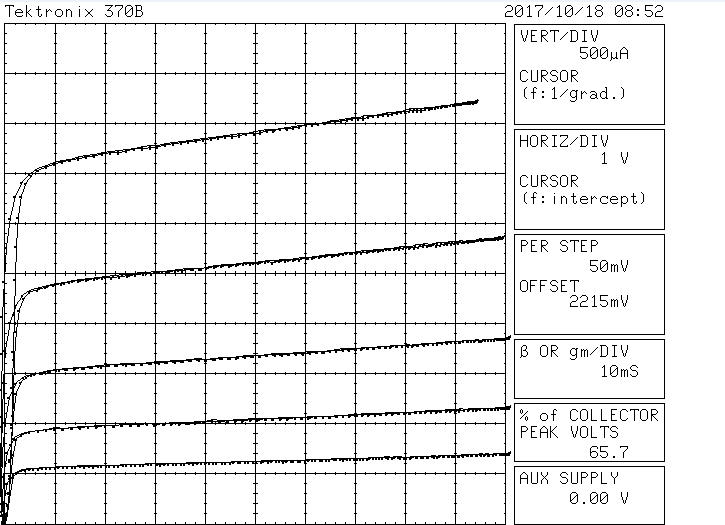


**Figure 12.** Circuit configuration for the Rout measurement for the first stage of the circuit

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Parameter | Spec & Limits | Calcs | Sim | %Error |
| ID (mA) | ≤ 75% max transistor DC current | 1.28m | 1.23m | 3.91 |
| Avo (V/V) | N/A | N/A | -19.23 | N/A |
| Av (V/V) | -3 V/V ≥ AV ≥ -30 V/V | -19.13 | -18.91 | 1.15 |
| Gv (V/V) | N/A | N/A | -18.34 | N/A |
| Rin (kΩ) | ≥ 100 kΩ | 132.2k | 132.2k | 0 |
| Rout (kΩ) | ≤ 5 kΩ | 4.7k | 4.7k | 0 |
| PD (mW) | ≤ 75% of max power any part | 7.68m | 7.64m | 0.39 |

**Table 5.** Comparison of calculated circuit values to the simulated values

Multisim simulation can’t come up with accurate values without using an approximate value for k and Vt. Using the curve tracer, a transistor can be characterized for more accurate values of k and Vt.



**Figure 13.** A Screenshot of the curve tracer characterizing BS-170

Biasing Scheme:

VDD = 15V

VD  = 0V, VS = 7 V

Set drain current to 60 mA and calculate for VOV

Choose ID = 60 mA:

VOV = +/- 0.693V

Saturation:

1. Vov = VG − VS − Vt = 0.693 V 2) Vov = VG − VS − Vt = −0.693 V Vov = VG − 6V − 2V = 0.693 V Vov = VG − 6V − 2V = −0.693 V VG = 5.693 V VG = 4.307 V VGS = -1.307 V VGS = -2.693 V |VGS| <|Vt| |VGS| <|Vt| Transistor is off Transistor is on

Calculating gm:

gm = kVov

gm = (250mA/V2 )(0.693V)

gm = 173.25mA/V

Calculating Resistors:

RS3 = (15V – 7V)/(60mA)

RS3 = 133.3

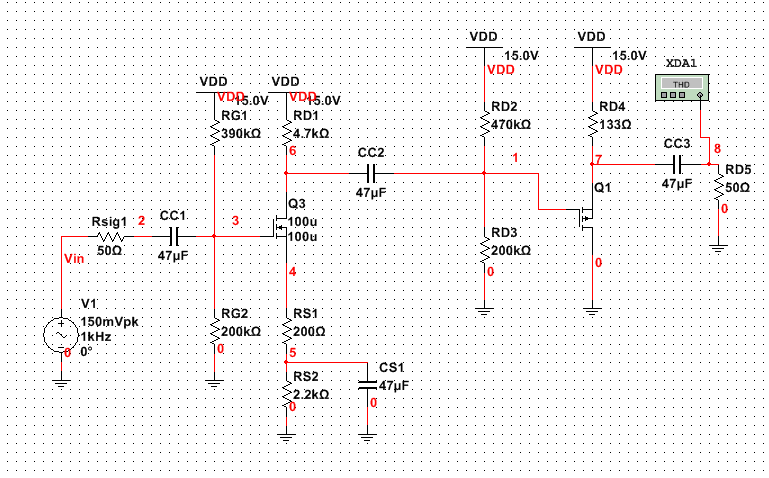
Let RG4 equal 200kΩ, then RG3 equals 497kΩ.

Calculating Av:

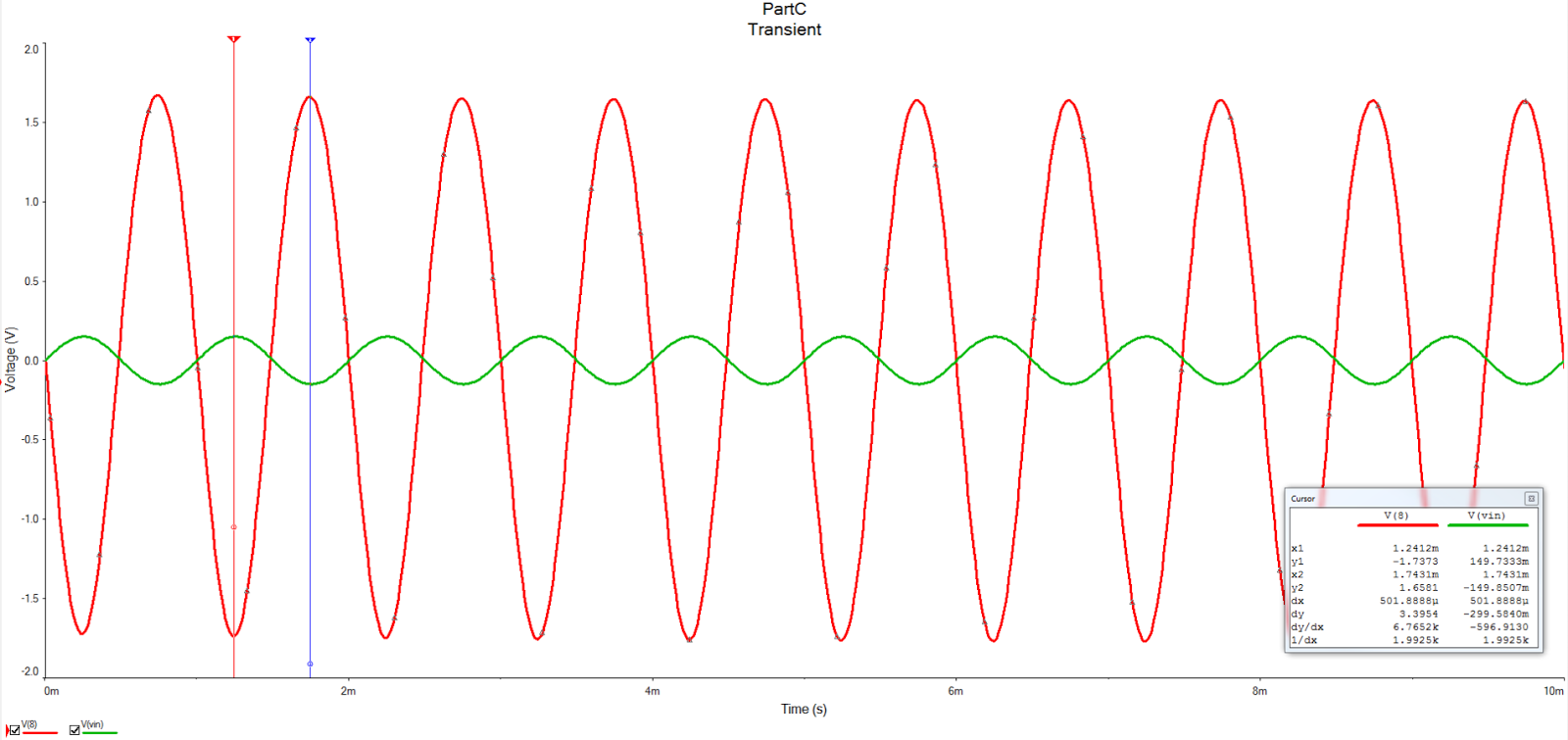
Av = 0.863 V/V

Calculating AV0:

Calculating GV:



**Figure 14.** Cascaded Amplifier added to Single Stage Amplifier

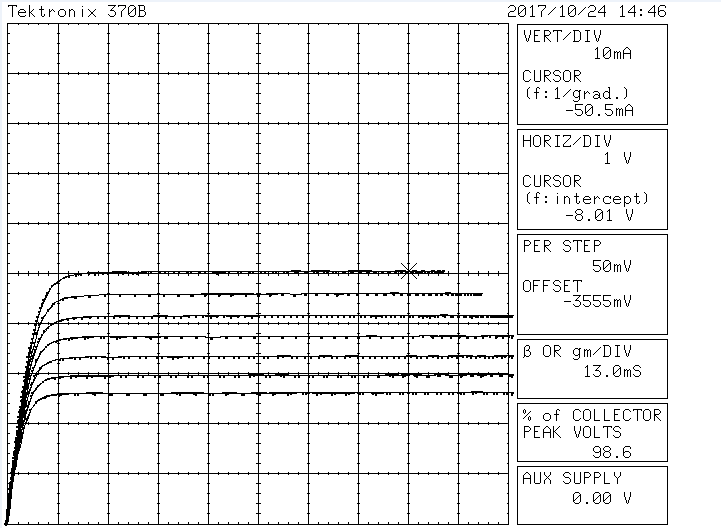


**Figure 15.** Simulated waveform for the Av gain of the Cascaded Amplifier

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Parameter | Spec & Limits | Calcs | Sim | %Error |
| ID (mA) | ≤ 75% max transistor DC current | 60m | 56.9m | 5.16 |
| Avo (V/V) | For the CD amplifier only | N/A | 0.7705 | N/A |
| Av (V/V) | For the CD amplifier only | 0.863 | 0.7705 | 10.72 |
| Gv (V/V) | For the CD amplifier only | N/A | 0.7702 | N/A |
| Rin (kΩ) | ≥ 100 kΩ | 143k | 143k | 0 |
| Rout (kΩ) | ≤ 5 kΩ | 5.53 | 10.01 | 81 |
| PD (mW) | ≤ 75% of max power any part | 127m | 113m | 11 |

**Table 6.** Simulated parameter values for the second stage of the circuit

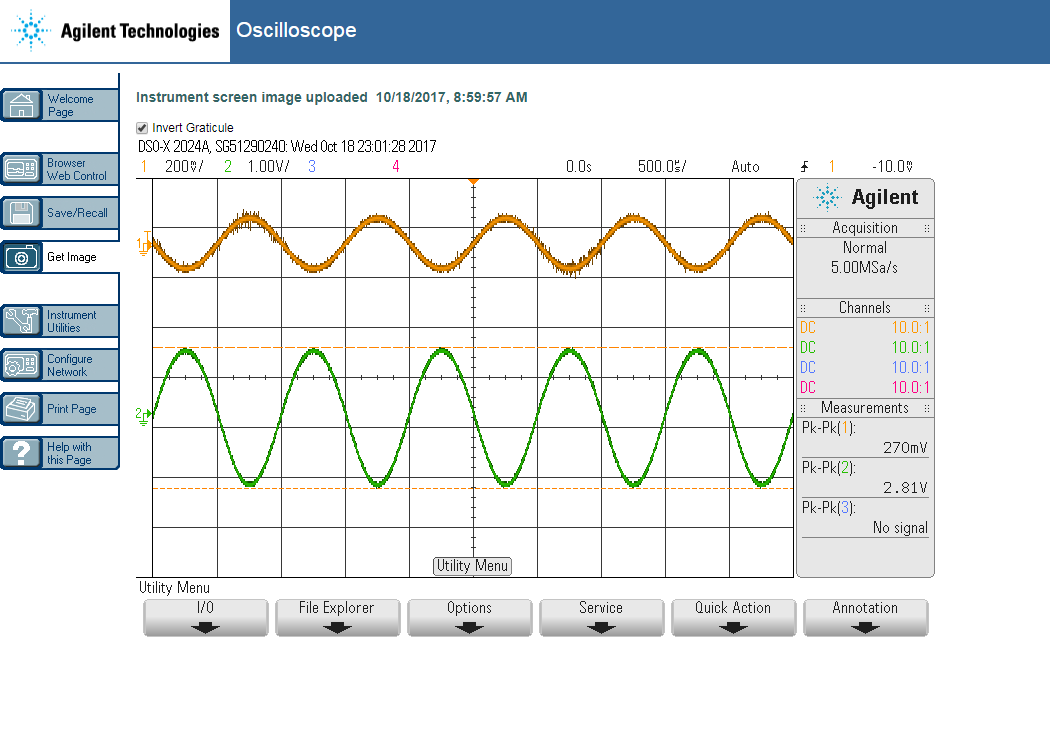
Multisim simulation can’t come up with an accurate value without using an approximate values for k and Vt. Using the curve tracer, a transistor can be characterized for more accurate values of k and Vt.



**Figure 16.** A Screenshot of the curve tracer characterizing BS-270

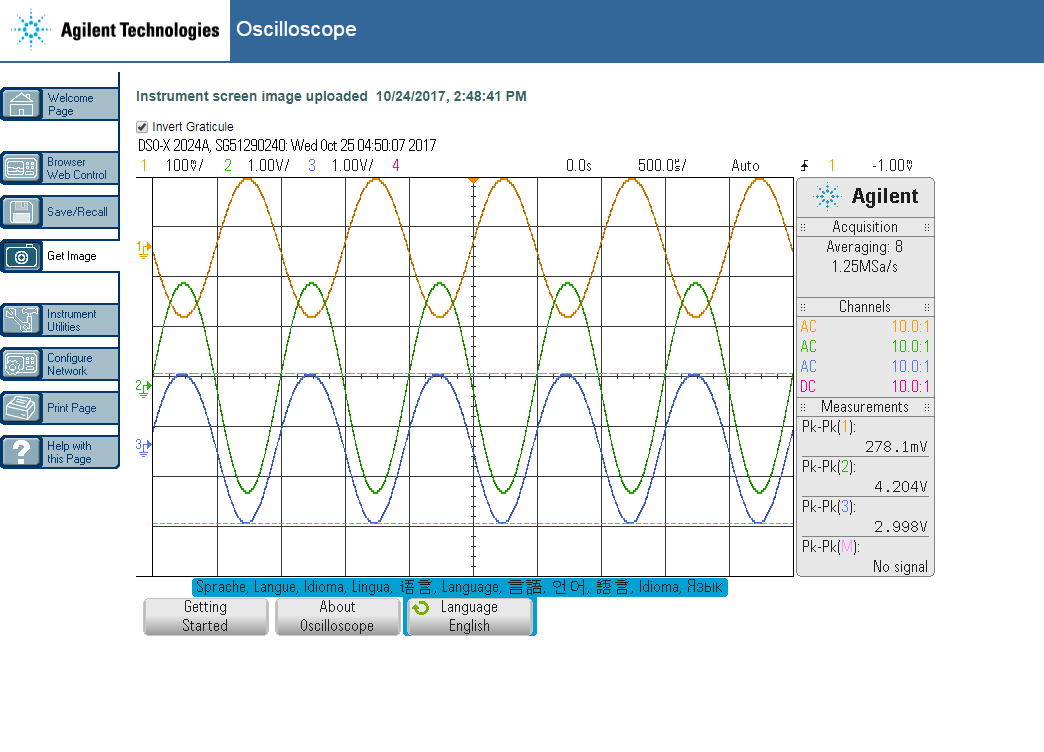
**Implementation**

With the construction of the circuit, the most common source of error was introduced. With the Multisim schematics, using real resistor values, as a reference, the circuit for Part A was built identically. The oscilloscope was used to determine the effectiveness of the amplifier, with channel 1 connected to the node at the transistor’s gate, measuring input amplitude, and channel 2 connected to the node at the load resistor.



**Figure 17.** Oscilloscope Reading for Av, showing gain specification.

Since the gain of greater than 3V has been verified, the cascaded amplifier can be implemented. Unlike the single-stage amplifier for Part A, the drain resistance had to be divided among three serial resistors (33Ω, 47Ω, and 51Ω) in order to prevent an excessive dissipation of power. With this exception, the circuit was built as shown in the Multisim schematic. The oscilloscope was connected in the same places for stage 1, channel 2 relocated just after the first transistor, with the addition of channel 3 connected at the node before the new load resistor.



**Figure 18.** Oscilloscope reading for Av, showing gain for stage 1 and stage 2.

**Analysis and Testing**

After the implementation of the cascaded amplifier, various analysis was conducted in order to verify that it met specifications and behaved as designed. The oscilloscope was used to measure gain, Rin and Rout, and ID. The results can be found below in Table 7.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Parameter | Spec & Limits | Sim | Lab | %Error |
| ID (mA) | ≤ 75% max transistor DC current | 1.17m | 0.88m | 24.79 |
| Avo (V/V) | N/A | -12.05 | -12.74 | 5.73 |
| Av (V/V) | -3 V/V ≥ AV ≥ -30 V/V | -11.51 | -11.71 | 1.74 |
| Gv (V/V) | N/A | -18.34 | \*Can't | Measure |
| Rin (kΩ) | ≥ 100 kΩ | 132.2k | 129.7k | 1.89 |
| Rout (kΩ) | ≤ 5 kΩ | 4.7k | 4.61k | 2.13 |
| PD (mW) | ≤ 75% of max power any part | 7.68m | 4.65m | 39.5 |

**Table 7.** Results from lab readings and Multisim data for Stage 1

While all of the parameters are within required specifications and limits, there are some large errors between the simulation and the measured values. The error between most parameters falls within a tolerable range, but ID sticks out with a large deviance between the simulation and measured value. This can most likely be attributed to a slight modeling error, and a large human error with part selection and real resistor values.

For stage 2, the oscilloscope was used to gather the same data, shown below in Table 8.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Parameter | Spec & Limits | Sim | Lab | %Error |
| ID (mA) | ≤ 75% max transistor DC current | 56.9m | 51m | 10 |
| Avo (V/V) | For the CD amplifier only | 0.7705 | 1.072 | 39.13 |
| Av (V/V) | For the CD amplifier only | 0.7705 | 0.7668 | .5 |
| Gv (V/V) | For the CD amplifier only | 0.7702 | N/A | N/A |
| Rin (kΩ) | ≥ 100 kΩ | 143k | 138.85k | 2.90 |
| Rout (kΩ) | ≤ 5 kΩ | 10.01 | 13.16 | 31.5 |
| PD (mW) | ≤ 75% of max power any part | 113m | 122m | 7.96 |

**Table 8.** Results from lab readings and Multisim data for Stage 2

For stage 2, the required specifications and limits were also met, but again there are some large differences between the simulation and measured results. The most glaring discrepancies are for Avo and Rout. Part of the error for both of these values may be compounded error from the separate stages of the amplifier and variance in part selection. A large portion of this error can be attributed to modeling error, using an approximate value for gm and other transistor characteristics in the simulation. Moreover, the error in Rout will directly contribute to the error in Avo­.

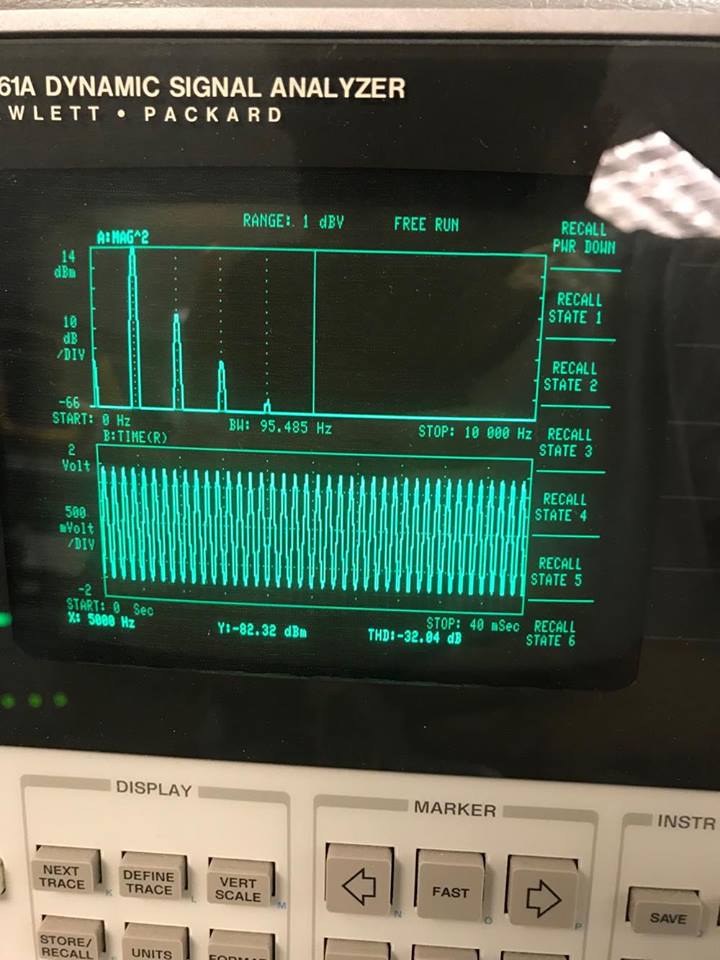
1) Why can the new configuration achieve the desired Av into the 50 Ω load when the common-source amplifier of Part A by itself cannot?

2) How low can RL get and still have a non-distorted output (symmetrical about zero volts and/or not clipped)?

3) What could you change in the new circuit to achieve the correct output into a smaller RL? Note: Don’t actually do this on the real circuit as you might exceed wattage rating. Just simulate results in Multisim.

4) What would happen to the total circuit gain if the Rin of the pMOS (Source Follower) was ≤ 100 kΩ

Bonus:



**Figure 19.** Distortion Analysis of the Cascaded Amplifier

We found the distortion of the amplifier by using the signal analyzer. We put the probes across the 50 ohms resistor for Rload. As you can see we have distortion less than -31 dB, which is lower than the instructor's. We measured -32.04 dB. In order to get this value, we increased the VDD. We had to be careful about not burning a resistor, but everything went well.

**Conclusions**

The amplifier functioned as designed and met all specifications. While the amplifier did not function exactly as designed, this can be attributed to modeling error with hand calculations. The equations used to design the stages of the amplifier make numerous assumptions that could have caused this deviation. Another potential source of error is the noise on the signal, which may have prevented an accurate reading of values on the oscilloscope. Nonetheless, all requirements and specifications were met. One of the biggest takeaways from this lab is how an amplifier works and the design principles behind it. An amplifier is a very common electronic component, used in a number of everyday applications. This lab also highlighted one of the central applications of the transistor and furthered our understanding of its function and purpose. Furthermore, the main purpose in cascading these two transistor circuits, the second of which reduces gain, is to allow for a smaller load resistance. This allowed for a deeper understanding of the difference between n- and p-MOS transistors and their function.

Documentation: Revised by C2C Luke McFadden